Amendments to the Claims

1. (CURRENTLY AMENDED) An electronic device ~~(70)~~ comprising a TFT ~~(9,59)~~, the TFT including a channel ~~(16)~~ defined in a layer of polycrystalline semiconductor material ~~(10,48)~~ produced by crystallising amorphous semiconductor material ~~(2,44)~~ using metal atoms ~~(6)~~ to promote the crystallisation process, wherein the semiconductor material includes an average concentration of the metal atoms in the range $1.3x10^{18}$ to $7.5x10^{18}$ atoms/cm^3.

2. (ORIGINAL) An electronic device of Claim 1 wherein the average concentration of the metal atoms in the semiconductor material is around $2.5x10^{18}$ atoms/cm^3.

3. (CURRENTLY AMENDED) An electronic device of ~~Claim 1 or Claim 2~~Claim 1 wherein the TFT ~~(59)~~ has a bottom gate configuration.

4. (CURRENTLY AMENDED) An electronic device of Claim 3 wherein the gate electrode ~~(40)~~ of the TFT ~~(59)~~ comprises a metallic material.

5. (CURRENTLY AMENDED) An electronic device of ~~any preceding Claim~~Claim 1 wherein the gate electrode ~~(40)~~ of the TFT ~~(59)~~ comprises a metal silicide.

6. (CURRENTLY AMENDED) An electronic device of ~~any preceding Claim~~Claim 1 wherein the gate electrode ~~(40)~~ comprises semiconductor material and metal atoms suitable for promoting the crystallisation thereof.

7. (CURRENTLY AMENDED) A method of manufacturing an electronic device including the steps of:

(a) depositing amorphous semiconductor material ~~(2,44)~~ on a substrate ~~(4)~~;

(b) adding metal atoms ~~(6)~~ to the semiconductor material at an average concentration therein in the range $1.3x10^{18}$ to $4x10^{18}$ atoms/cm^3, the metal atoms

being suitable for accelerating the crystallisation of amorphous semiconductor material; and

(c) annealing the amorphous semiconductor material to form polycrystalline semiconductor material.

8. (CURRENTLY AMENDED) A method of Claim 7 wherein the metal atoms ~~(6)~~ are added to the amorphous semiconductor material at an average concentration therein of around $2.5x10^{18}$ atoms/cm^3.

9. (CURRENTLY AMENDED) A method of Claim 7 or Claim 8 wherein the metal atoms ~~(6)~~ are added by implantation.

10. (CURRENTLY AMENDED) A method of ~~any of Claims 7 to 9~~Claim 7 wherein the annealing process is carried out for 10 hours or less at a temperature of 600°C or less, and a TFT ~~(9,59)~~ is formed with its channel defined in the polycrystalline semiconductor material which exhibits a minimum leakage current of around $2.5x10^{-12}$ A/μm or less at a source-drain voltage of 5V.

11. (CURRENTLY AMENDED) A method of Claim 10 wherein the annealing process is carried out for 8 hours or less at a temperature of 550°C or less, and a TFT ~~(9,59)~~ is formed with its channel defined in the polycrystalline semiconductor material which exhibits a minimum leakage current of around $2.5x10^{-12}$ A/μm or less at a source-drain voltage of 5V.

12. (CURRENTLY AMENDED) A method of ~~any of Claims 7 to 11~~Claim 7 wherein a TFT ~~(59)~~ is formed with its channel defined in the polycrystalline semiconductor material which has a bottom gate configuration, the method comprising a back channel etch step.

13. (CURRENTLY AMENDED) An electronic device of ~~any of Claims 1 to 6~~Claim 1 or a method of ~~any of Claims 7 to 12~~Claim 7 wherein the metal atoms ~~(6)~~ comprise nickel atoms.

14. (CURRENTLY AMENDED) An active matrix display device ~~(68)~~ wherein an electronic device ~~(70)~~ of ~~any of Claims 1 to 6 or Claim 13~~Claim 1 forms the active plate of the active matrix device.